

(Translation)

**NOTIFICATION OF REASONS FOR REJECTION**

Date of Issue: November 26, 2003

Patent Application No.: 091125094

Filing Date: October 25, 2002

Applicant: Kabushiki Kaisha Toshiba

Title of Invention: Variable displacement condenser and amplifier applied to a semiconductor device

Basis for rejection: Section 20(2) of the Patent Law

**Reasons:**

- (1) The "variable displacement condenser and amplifier applied to a semiconductor device" of the present application provide a semiconductor which reduces the resistance of a base part of a well region in a substrate. The present invention is characterized in that it is possible to reduce the resistance between a first conductive well region and a second conductive well region by implanting a high concentration ion into the base part of the well region.
- (2) The technology of the present invention is a well known technology in which a low resistance region is formed in the base part of a well region by implantation of a high concentration ion. For example, Chinese Patent Publication No. 409353 (published on October 21, 2000) regarding "a manufacturing process of a metal contact to reduce contact resistance and a metal contact forming a transistor using the manufacturing process" (refer to the attached Reference) discloses implanting a high concentration ion into a region and reducing contact between the contact parts. Therefore, comparing the present invention and the invention disclosed in the Reference, both define a method in which the resistance effect between

contact parts are reduced by implanting a high concentration ion into the region. The difference between the two inventions is that the structure of the semiconductors used are different. The difference can easily be conceived from the Reference and the present invention can be performed. Thus, the present application does not possess an inventive step.

- (3) Summarizing the above, a person skilled in the art can easily perform the present invention by applying the technology or knowledge already existing before the present application, and it is difficult to say that the application satisfies the requirement of a patent.

Based on the above conclusion, the present application does not satisfy the requirement provided in the Patent Law (Section 20(2) of the Patent Law).

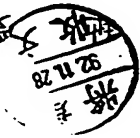
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經濟部智慧財產局專利核駁審定書

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發文日期：中華民國九十二年十一月二十六日  
 發文字號：九二(二)智專(一)第06050號  
 第一、申請案號：九二〇九一二二九九三〇〇號  
 第二、發明名稱：適用於可變容量電容器及放大器的半導體裝置

專利分類IPC(7).....H01L 27/08

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[illegible]

(二) 本案的技術在於利用高濃度離子佈植摻雜井區底部以形成低電阻區域，惟利用高摻雜

(一) 本「案」適用於可變電容器及放大器的半導體裝置提供一種降低基板內底部導電阻的半導體裝置，其特徵為：利用高濃度離子佈植摻雜井區底部，可以降低第一導電

甲

依據：專利法第二十一條第二項。

主文：本案應不予專利。

## 八、審定内容：

七、審查人員姓名：謝志偉 委員

1 2001/12/27 □ 2001-398386

## 六、優先權項目：

五、申請日期：九十年十二月二十五日



五十頁計，向本局申請再審查。

整（專利說明書及圖式合計在五十頁以上者，每五十頁加收新台幣五百元，其不足五十頁者以整如不服本審定，得於文到之次日起三十日內，備具再審查理由書一式二份及規費新台幣陸仟元依照分層負責規定授權單位主管決行

# 蔡 練 生 局長

據上論結，本案不符合法定專利要件，爰依專利法第二十二條第二項，審定如主文。

者，難謂符合發明專利要件。

（三）綜上所述，本案係運用申請前既有之技術或知識，而為熟習該項技術者所能輕易完成，該差異處可由引證案輕易知悉並完成，並無顯著進步之處，故本案不具進步性。植摻雜區域，以達到降低接觸點間的電阻效果，其差異處僅在使用的半導體結構不同